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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,591	07/16/2003	Shih-Hsien Wu	3313-1016P	7448

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EXAMINER	
NADAV, ORI	
ART UNIT	**PAPER NUMBER**
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/04/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 04/04/2007.

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mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/619,591	WU ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,14-24 and 26-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,14-24 and 26-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7-11, 14-18, 20-24, 26-30 and 32-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berger et al. (6,528,145) in view Nishide et al. (5,827,605), Zak (6,006,427) and Hashemi et al. (6,867,493).

Berger et al. in figure 3 and related text a composite laminate substrate, comprising:

at least an inorganic substrate 20 having at least a wiring 26 formed thereon; and

two substrates, comprising print circuit boards (column 10, lines 32-45 and column 12, lines 44-46) integrated with the at least an inorganic substrate, having circuits for electrical connections between outer input/output ports and said wiring of said inorganic substrate through said print circuit boards (substrates).

Berger et al. do not teach the print circuit boards being organic print circuit boards and at least a passive component formed in/on the inorganic substrate, and at least one bonding layer having vias formed therein, for bonding said inorganic substrate and said print circuit board (substrate).

Nishide et al. teach in figure 1 and related text an inorganic substrate 1, 2 having at least a passive component 4, 5, 8 selected from a group consisting of capacitor,

inductor and resistor, formed therein/thereon, and circuits for electrical connections between outer input/output ports and said passive component of said inorganic substrate.

Zak teaches print circuit boards being organic print circuit boards, and the advantages of using organic print circuit boards (column 2, lines 40-45).

Hashemi et al. teach in figure 8 and related text at least one bonding layer 815 having vias 853 formed therein, for bonding substrate 820 and a print circuit board 898.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use organic print circuit boards and at least a passive component formed on the inorganic substrate in Berger et al.'s device, such that two organic substrates, located on two sides of said inorganic substrate, having electrical connections between outer input/output ports and said passive component of said inorganic substrate through said organic substrates, and at least one bonding layer having vias for bonding said inorganic substrate and said print circuit board (substrate), in order to reduce the cost of making the device and in order to make more compact device by forming the two organic substrates on both sides of said inorganic substrate and by forming the passive elements within the inorganic substrate, and in order to provide more solid connection between the inorganic substrate and the print circuit board, respectively.

Regarding claims 2, 15 and 27, prior art teaches the material of said inorganic substrate is selected from the group consisting of ceramic, silicon and glass.

Regarding the process limitations recited in claims 3-4, 7-8, 11, 16-17, 20-21, 24, 28-29, 32-33 and 36 ("passive component is made from the process selected from the group consisting of thick film process and thin film process", "passive component is made from a semiconductor fabrication process", "the circuit of the print circuit boards are made separately, and then stacked together to form said organic substrates, " the circuit of the print circuit boards are made separately, then stack the print circuit boards together, and finally form the circuit of a surface layer with build-up process to form said organic substrates", and "wherein said organic substrate is made on said inorganic substrate with build-up process", .these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 9-10, 22-23 and 34-35, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use at least a passive component on said organic substrate and selected from a group consisting of capacitor, inductor and resistor in prior art's device in order to the device in an application which requires a passive element.

Regarding claim 26, Hashemi et al. teach in figure 8 and related text at least one bonding layer 815 having vias 853 formed therein, for bonding substrate 820 and a print circuit board 898. Said covering layer meets the claimed limitations of a covering layer, for covering said inorganic substrate and bonding to said organic substrate such that said inorganic substrate covered by said covering layer is integrated between said organic substrates, and said covering layer further comprising circuits 815 for providing electrical connections between said passive component and said organic substrate.

Claims 6,19 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berger et al., Nishide et al., Zak and Hashemi et al., as applied to claims 1 and 14 above, and further in view of Czjakowski et al. (6,613,978).

Berger et al., Nishide et al., Zak and Hashemi et al. teach substantially the entire claimed structure, as applied to claims 1 and 14 above, except each of said organic substrate is composed of a plurality of print circuit boards.

Czjakowski et al. teach a plurality of print circuit boards formed on a ceramic substrate.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form each of said organic substrate of a plurality of print circuit boards, in prior art's device in order to use the device in an application which requires plurality of print circuit boards.

Response to Arguments

Applicant argues that there is no motivation to combine the references, because even if the cost of making the device would be reduced and the device would be more compact, this is not sufficient motivation for one skilled in the art to look to other references to change the Berger et al. device without some need to do so.

It is unclear to the examiner why reducing the cost of the device is not sufficient motivation for one skilled in the art to look to other references.

Applicant argues that in the present invention, the bonding layer only provides bonding between two substrates of different materials and does not provide electrical interconnection between two substrates, and the electrical connection is connected by via holes, buried holes or blind holes, whereas the BGA of Berger et al. provides an electrical between substrates and components and the BGA technology is not suitable for bonding of organic or inorganic substrates due to the degradation of the ball grid array by room temperature aging.

The examiner does not suggest bonding the substrates using BGA technology. The examiner suggests that an artisan would use Hashemi et al.'s teaching of bonding substrate 820 and a print circuit board 898 by using bonding layer 815.

Furthermore, Berger et al. do not teach that BGA technology should be used to bond the substrates. Berger et al. state that BGA is only one possible technology to bond the substrates. "The connections to the PCB can be made by using conventional surface mount technology such as ball grid arrays (BGA), land grid arrays (LGA) or pluggable interconnections."

Applicant argues that "The Examiner has relied on Nishide et al. to show an inorganic substrate with a passive component. The Examiner relies on Zak to show the advantages of an organic printed circuit board. The Examiner relies on Hashemi et al to show the vias. Applicants submit that the even if these references are combined they do not teach the present claimed invention since it is not clear how these various pieces could be put together into a single device in a workable fashion."

Although the examiner used three secondary references, Nishide et al., Zak and Hashemi et al. teach elements which are conventionally used in the art. The inclusion of a passive component in a substrate, as taught by Nishide, is broadly used in the art. The advantages of using an organic printed circuit board, as taught by Zak, provide the motivation to combine the references. The formation of vias, as taught by Hashemi et al., is the most widely used method of interconnection. Therefore, it would be clear to

an artisan how these various pieces could be put together into a single device in a workable fashion.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
3/29/07

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